An introduction to the memory-distributed aspect of the code Arpege/Ifs/Aladin

R. El Khatib
Météo-France - CNRM/GMAP
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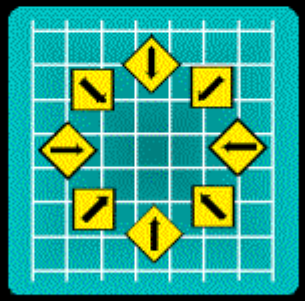
Introduction

- Law : T = s + P/n
  - n → Number of processors
  - P → Total CPU time in *parallel* part
  - s → Total CPU time in *serial* part
  - T → *Elapsed* CPU time

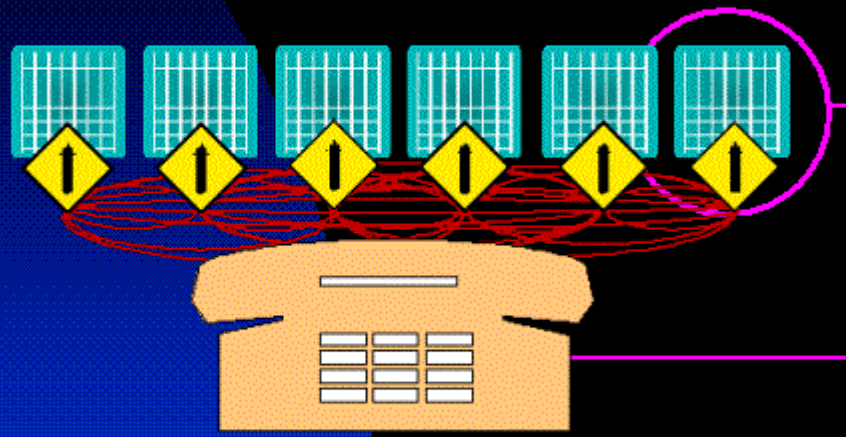
- Shared memory architecture :
  - * Several processors (yellow items)
  - * Shared-access central memory (blue area)



When the number of processors get huge,
The performance collapses
Because the memory access conflicts get preponderent !

Distributed memory architecture

- A machine divided per *nodes* :



A *node*

=

A processor

+

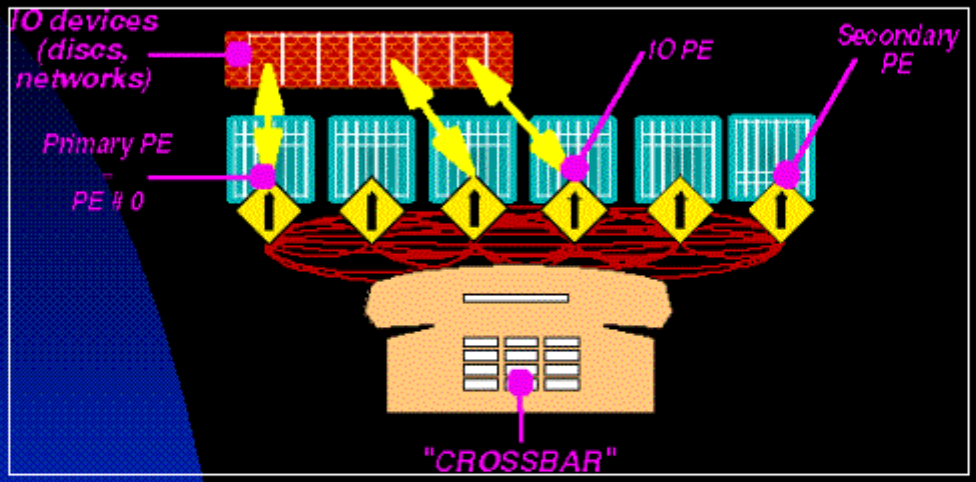
A piece of central memory

Inter-nodes communication system : « crossbar »

Possibility to build machines with up to 1000 or 2000 processors

Communications between nodes to be coded by the programmer

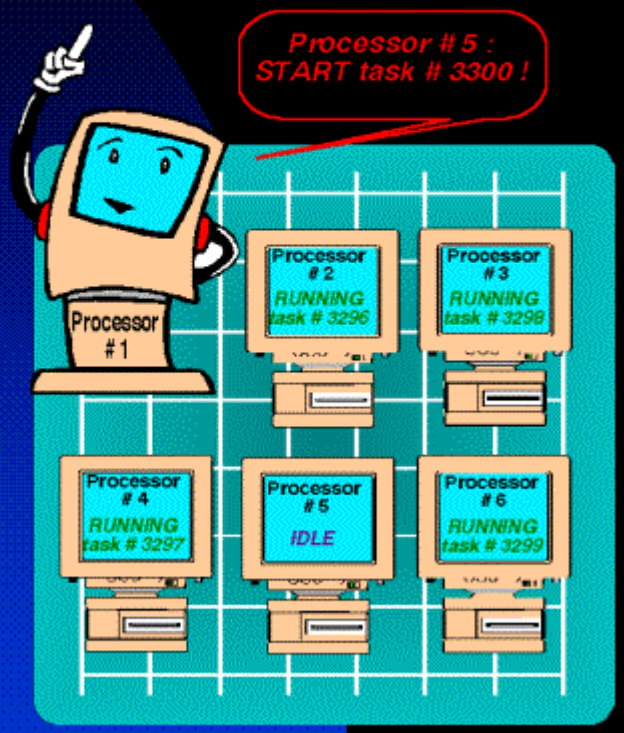
More about DM architecture



- Memory larger, cheaper …and slower
- Communications to be handled
- Calculation unit : scalar or vector processor

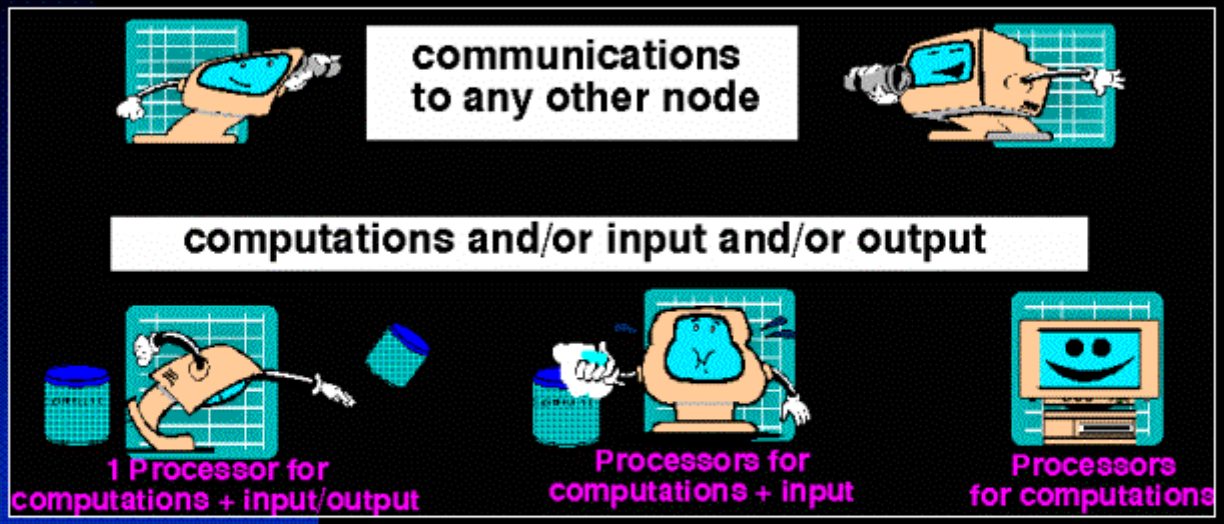
Incoming supercomputers : calculation unit = cluster of scalar processors

Multitasking



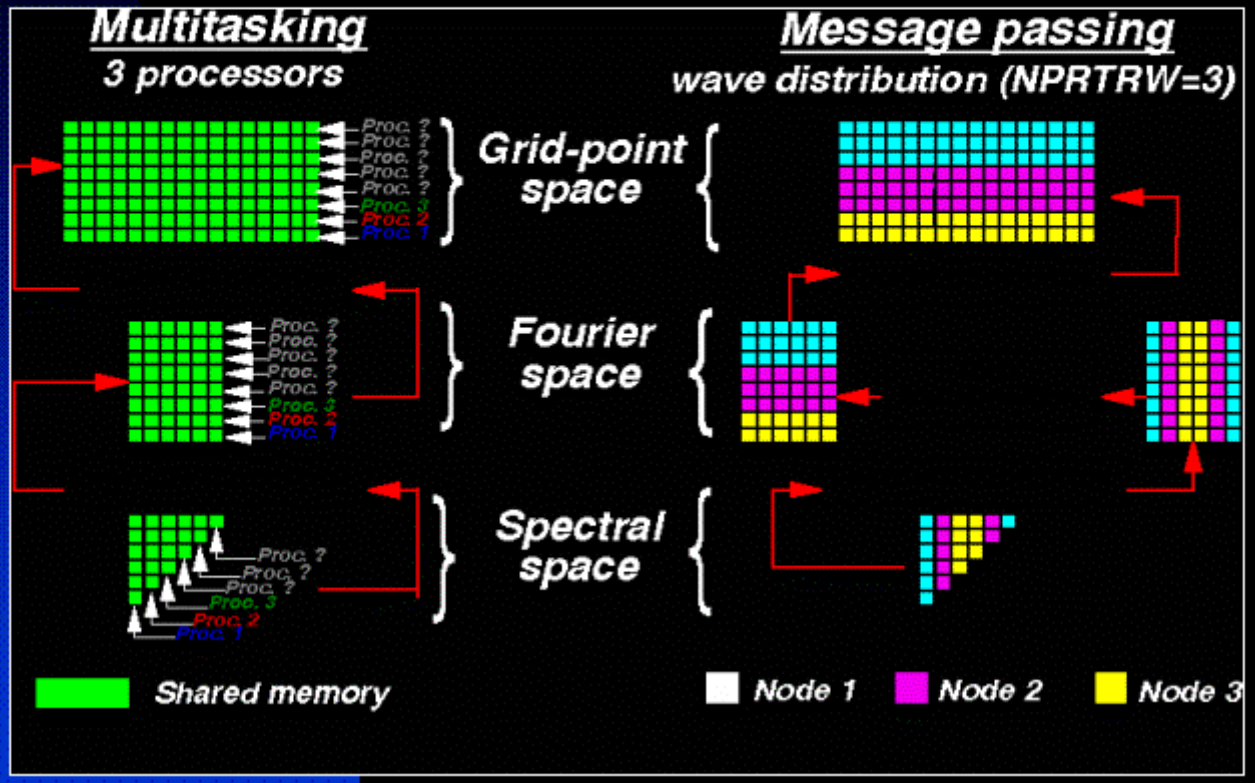
- One master-processor executing the serial code
- Slave-processors activated on specific tasks by the master-processor

Message passing

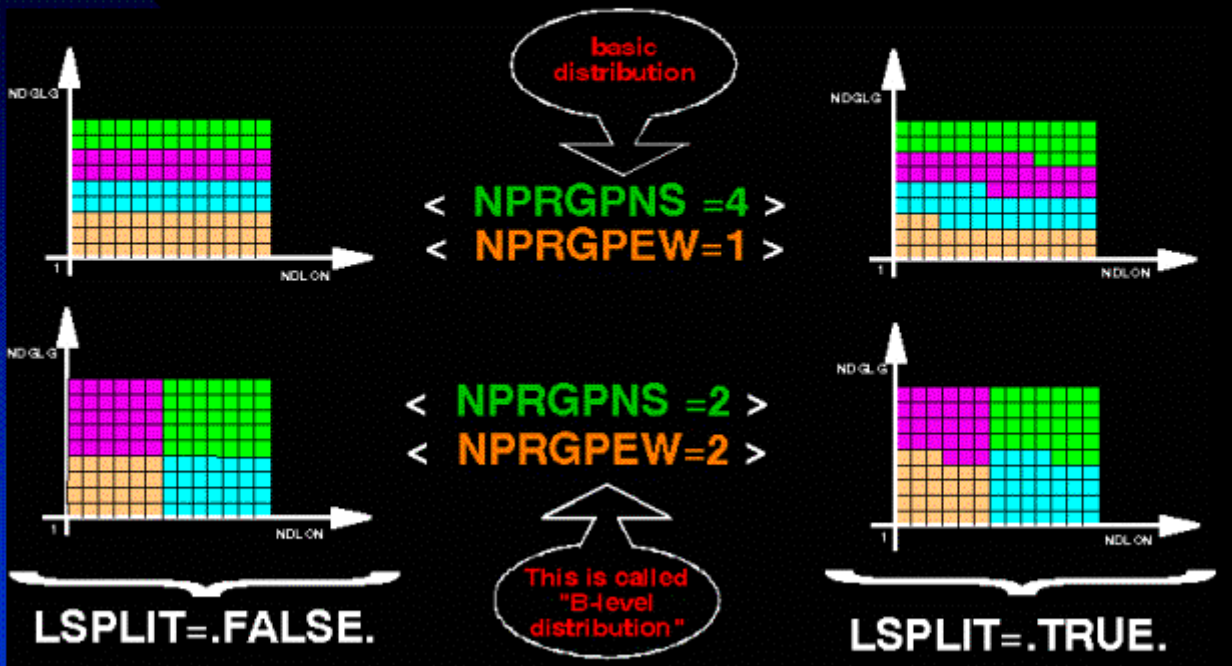


- Processors running through the whole code
- But not executing the whole code
- Communications involved

Spectral data distribution



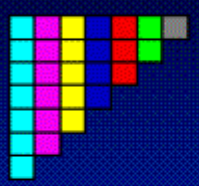
Gridpoint data distribution



« B-level » distribution

Example :

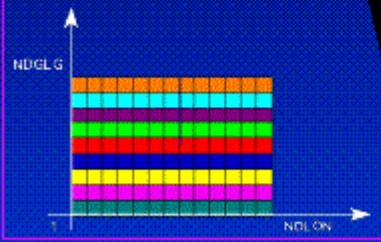
Truncation, 41 levels, TI298, reduced grid 300 latitudes x 600 longitudes



In spectral space = vertical level distribution

« A »-level : up to 298 processors

« A » + « B » levels : up to 298x41=12 218 processors



In gridpoint space = longitudes distribution

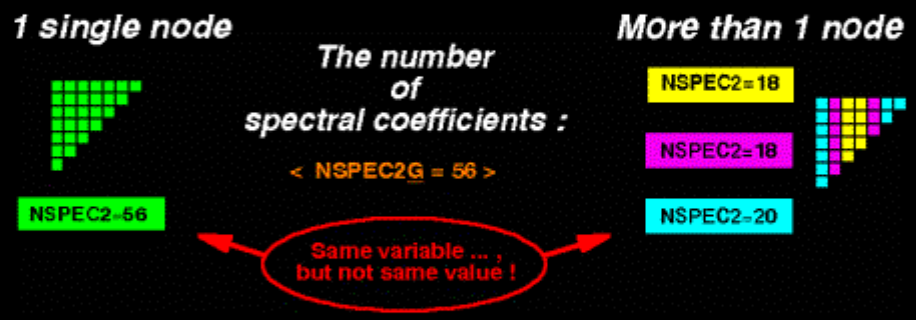
« A »-level : up to 300 processors

« A » + « B » levels : up to 126 596 processors

The « B-level » distribution enables us to reach the limits of the most powerful computers of today

Consequenses in the code

- New control keys
- *Local* versus *global* variables :



- *KEEP THE DISTRIBUTION SPIRIT IN MIND*
- *BEWARE OF THE PAST OF THE CODE (Shared memory heritage)*